



cof

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

August 1, 2006
Date

Alexandra Beggs
Alexandra Beggs

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Kie Y. Ahn and Leonard Forbes Attorney Docket No.: 500466.02
Patent No. : US 6,835,111 B2 Serial No. : 09/994,511
Issue Date : December 28, 2004 Filed : November 26, 2001
Title : FIELD EMISSION DISPLAY HAVING POROUS SILICON DIOXIDE LAYER

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**Certificate
AUG 10 2006
of Correction**

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56), References Cited, Litovchenko Reference	"IEEE International Conf. On Plasma Science,"	--IEEE International Conf. on Plasma Science,--
Item (56), References Cited, Vaudaine Reference	"technical digest of IEDM 91,"	--Technical Digest of IEDM 91,--
Column 1, Line 11	"displays, and,"	--displays and,--

AUG 14 2006

Column 3, Line 52	"n-type Silicon"	--N-Type Silicon--
Column 3, Line 55	"increasing ND"	--increasing N _D --
Column 4, Line 24	"IEEE E1."	--IEEE E1.--
Column 5, Line 5	"limiting, and"	--limiting and--
Column 6, Line 16	"from a normal"	--from normal--
Column 6, Line 31	"Mechanisms In"	--Mechanisms in--
Column 6, Line 39	"the ITO-P Inter SiO Intermediate Layer"	--the ITO-P Interface in α -Si:H Solar Cells Using a Thin SiO Intermediate Layer"--
Column 7, Line 20	"69(7), (1996), pp. 916-918."	--69(7) (1996), pp. 916-918.--
Column 7, Line 35	"Silicon at low"	--Silicon at Low--
Column 7, Line 57	"emitters 30', in a step"	--emitters 30' in a step--
Column 9, Line 63	"forms porous silicon"	--forms a porous silicon--
Column 10, Line 8	"A method of claim 19"	--The method of claim 19--
Column 10, Line 26	"wherein the act or forming"	--wherein the act of forming--
Column 10, Line 34	"The method of claim 22"	--The method of claim 22--
Column 10, Line 42	"The method of claim 22"	--The method of claim 22--
Column 10, Line 44	"layer at temperature"	--layer at a temperature--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

AUG 14 2006

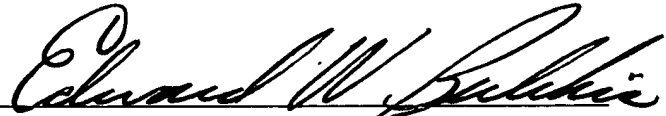
Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date:

July 31, 2006

By:



Edward W. Bulchis, Reg. No. 26,847

Customer No. 27,076

Dorsey & Whitney LLP

1420 Fifth Avenue, Suite 3400

Seattle, WA 98101

(206) 903-8785

Attorney for Applicant(s)

EWB:tdp

Enclosures:

Postcard

Form PTO-1050 (+ copy)

h:\ip\clients\micron technology\400\500466.02\500466.02 req cert correct.doc

AUG 14 2006



PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

August 1, 2006
Date

Alexandra Beggs
Alexandra Beggs

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Kie Y. Ahn and Leonard Forbes Attorney Docket No.: 500466.02
Patent No. : US 6,835,111 B2 Serial No. : 09/994,511
Issue Date : December 28, 2004 Filed : November 26, 2001
Title : FIELD EMISSION DISPLAY HAVING POROUS SILICON DIOXIDE LAYER

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56), References Cited, Litovchenko Reference	"IEEE International Conf. On Plasma Science,"	--IEEE International Conf. on Plasma Science,--
Item (56), References Cited, Vaudaine Reference	"technical digest of IEDM 91,"	--Technical Digest of IEDM 91,--
Column 1, Line 11	"displays, and,"	--displays and,--

AUG 14 2006

Column 3, Line 52	"n-type Silicon"	--N-Type Silicon--
Column 3, Line 55	"increasing ND"	--increasing N _D --
Column 4, Line 24	"IEEE E1."	--IEEE E1.--
Column 5, Line 5	"limiting, and"	--limiting and--
Column 6, Line 16	"from a normal"	--from normal--
Column 6, Line 31	"Mechanisms In"	--Mechanisms in--
Column 6, Line 39	"the ITO-P Inter SiO Intermediate Layer""	--the ITO-P Interface in α -Si:H Solar Cells Using a Thin SiO Intermediate Layer"--
Column 7, Line 20	"69(7), (1996), pp. 916-918."	--69(7) (1996), pp. 916-918.--
Column 7, Line 35	"Silicon at low"	--Silicon at Low--
Column 7, Line 57	"emitters 30', in a step"	--emitters 30' in a step--
Column 9, Line 63	"forms porous silicon"	--forms a porous silicon--
Column 10, Line 8	"A method of claim 19"	--The method of claim 19--
Column 10, Line 26	"wherein the act or forming"	--wherein the act of forming--
Column 10, Line 34	"Tie method of claim 22"	--The method of claim 22--
Column 10, Line 42	"Tho method of claim 22"	--The method of claim 22--
Column 10, Line 44	"layer at temperature"	--layer at a temperature--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

AUG 14 2006

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date:

July 31, 2006

By:

Edward W. Bulchis

Edward W. Bulchis, Reg. No. 26,847

Customer No. 27,076

Dorsey & Whitney LLP

1420 Fifth Avenue, Suite 3400

Seattle, WA 98101

(206) 903-8785

Attorney for Applicant(s)

EWB:tdp

Enclosures:

Postcard

Form PTO-1050 (+ copy)

h:\ip\clients\micron technology\400\500466.02\500466.02 req cert correct.doc



UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : US 6,835,111 B2
DATED : December 28, 2004
INVENTOR(S) : Kie Y. Ahn and Leonard Forbes

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56), References Cited, Litovchenko Reference	"IEEE International Conf. On Plasma Science,"	--IEEE International Conf. on Plasma Science,- -
Item (56), References Cited, Vaudaine Reference	"technical digest of IEDM 91,"	--Technical Digest of IEDM 91,--
Column 1, Line 11	"displays, and,"	--displays and,--
Column 3, Line 52	"n-type Silicon"	--N-Type Silicon--
Column 3, Line 55	"increasing ND"	--increasing N _D --
Column 4, Line 24	"IEEE E1."	--IEEE E1.--
Column 5, Line 5	"limiting, and"	--limiting and--
Column 6, Line 16	"from a normal"	--from normal--
Column 6, Line 31	"Mechanisms In"	--Mechanisms in--
Column 6, Line 39	"the ITO-P Inter SiO Intermediate Layer""	--the ITO-P Interface in α -Si:H Solar Cells Using a Thin SiO Intermediate Layer"--
Column 7, Line 20	"69(7), (1996), pp. 916-918."	--69(7) (1996), pp. 916-918.--
Column 7, Line 35	"Silicon at low"	--Silicon at Low--
Column 7, Line 57	"emitters 30', in a step"	--emitters 30' in a step--
Column 9, Line 63	"forms porous silicon"	--forms a porous silicon--

AUG 14 2006

Column 10, Line 8	"A method of claim 19"	--The method of claim 19--
Column 10, Line 26	"wherein the act or forming"	--wherein the act of forming--
Column 10, Line 34	"The method of claim 22"	--The method of claim 22--
Column 10, Line 42	"The method of claim 22"	--The method of claim 22--
Column 10, Line 44	"layer at temperature"	--layer at a temperature--

MAILING ADDRESS OF SENDER:

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101

Patent No. US 6,835,111 B2

No. add'l. copies
 @ .30 per page



FORM PTO-1050 (REV. 3-82)

h:\ip\clients\micron technology\400\500466.02\500466.02 pto 1050.doc

AUG 14 2006

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

PATENT NO. : US 6,835,111 B2
DATED : December 28, 2004
INVENTOR(S) : Kie Y. Ahn and Leonard Forbes

It is certified that errors appear in the above identified patent and that said Letters Patent is hereby corrected as shown below:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56), References Cited, Litovchenko Reference	"IEEE International Conf. On Plasma Science,"	--IEEE International Conf. on Plasma Science,- -
Item (56), References Cited, Vaudaine Reference	"technical digest of IEDM 91,"	--Technical Digest of IEDM 91,--
Column 1, Line 11	"displays, and,"	--displays and,--
Column 3, Line 52	"n-type Silicon"	--N-Type Silicon--
Column 3, Line 55	"increasing ND"	--increasing N _D --
Column 4, Line 24	"IEEE E1."	--IEEE E1.--
Column 5, Line 5	"limiting, and"	--limiting and--
Column 6, Line 16	"from a normal"	--from normal--
Column 6, Line 31	"Mechanisms In"	--Mechanisms in--
Column 6, Line 39	"the ITO-P Inter SiO Intermediate Layer""	--the ITO-P Interface in α -Si:H Solar Cells Using a Thin SiO Intermediate Layer"--
Column 7, Line 20	"69(7), (1996), pp. 916-918."	--69(7) (1996), pp. 916-918.--
Column 7, Line 35	"Silicon at low"	--Silicon at Low--
Column 7, Line 57	"emitters 30', in a step"	--emitters 30' in a step--
Column 9, Line 63	"forms porous silicon"	--forms a porous silicon--

AUG 14 2005

Column 10, Line 8	"A method of claim 19"	--The method of claim 19--
Column 10, Line 26	"wherein the act or forming"	--wherein the act of forming--
Column 10, Line 34	"Tie method of claim 22"	--The method of claim 22--
Column 10, Line 42	"Tho method of claim 22"	--The method of claim 22--
Column 10, Line 44	"layer at temperature"	--layer at a temperature--

MAILING ADDRESS OF SENDER:

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101

Patent No. US 6,835,111 B2

No. add'l. copies

@ .30 per page



FORM PTO-1050 (REV. 3-82)

h:\ip\clients\micron technology\400\500466.02\500466.02 pto 1050.doc

AUG 14 2006